REMARKS

Claims 3-10 and 21-35 are pending in the present application. Claims 4, 10, 21 and 23-35 have been amended.

Claim Rejections-35 U.S.C. 103

Claims 3-10 and 21-35 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Itonaga reference (U.S. Patent Application Publication No. 2002/0061639) in view of the Yu et al. reference (U.S. Patent Application Publication No. 2003/0029715). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The method for fabricating a silicon on insulator semiconductor device of claim 21 includes in combination "subjecting the metallic silicide layer to a second heat treatment after said removing the protective layer, so that the metallic silicide layer has a low resistance crystalline structure and a sheet resistance of about 10 Ω/sq".

The Itonaga reference as relied upon by the Examiner is generally related to an MIS type semiconductor device formed on bulk substrate 1, as shown in Figs. 1A – 2C, for example. Although the Itonaga reference very generally describes in paragraph [0141] that the semiconductor substrate is not limited to a bulk semiconductor substrate as specifically described, but may alternatively be an SOI substrate, the Itonaga reference does not provide specific features and thus does not specifically disclose the method as for a silicon on insulator device. More particularly, the Itonaga reference

does not describe subjecting a metallic silicide layer of a silicon on insulator layer to a second heat treatment after removing a protective layer, so that the metallic silicide layer has a low resistance crystalline structure and a sheet resistance of about 10 Ω/sq, as would be necessary to meet the features of claim 21. The Yu et al. reference as secondarily relied upon does not overcome these deficiencies of the Itonaga reference. Applicant therefore respectfully submits that the method of fabricating a silicon on insulator semiconductor device of claim 21 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 4-10, 21 and 22, is improper for at least these reasons.

The method of manufacturing a silicon on insulator semiconductor device of claim 23 includes in combination "subjecting the first metallic silicide layer to a second heat treatment after said removing the protective layer, so as to change the first metallic silicide layer into a second metallic silicide layer having a low resistance crystalline structure and a thickness of 30 nm".

Applicant respectfully submits that the Itonaga reference as relied upon by the Examiner does not specifically describe in detail or disclose subjecting a first metallic silicide layer to a second heat treatment after removing a protective layer, so as to change the first metallic silicide layer into a second metallic silicide layer having a low resistance crystalline structure and a thickness of 30 nm, as would be necessary to meet the features of claim 23. The Yu et al. reference as secondarily relied upon does

not overcome these deficiencies of the Itonaga reference. Applicant therefore respectfully submits that the method of manufacturing a silicon on insulator semiconductor device of claim 23 would not have obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 23-29, is improper for at least these reasons.

The method of manufacturing a silicon on insulator semiconductor device of claim 30 includes in combination "forming a high resistance metallic silicide layer on the silicon layer under the protective layer by a first heat treatment whereby the substrate is heated to 750°C in a nitrogen gas atmosphere, the high resistance metallic silicide layer having a first crystalline structure".

The Itonaga reference describes in paragraph [0071] for example, a first rapid thermal annealing (RTA) at a temperature of about 400°C. The Itonaga reference does not describe a first heat treatment whereby the substrate is heated to 750°C in a nitrogen atmosphere, as would be necessary to meet the features of claim 30. The Yu et al. reference as secondarily relied upon does not overcome these deficiencies of the Itonaga reference. Applicant therefore respectfully submits that the method of manufacturing a silicon on insulator semiconductor device of claim 30 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 30-35, is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of three (3) months to May 8, 2006, for the period in which to file a response to the outstanding Office Action. The required fee of $1020.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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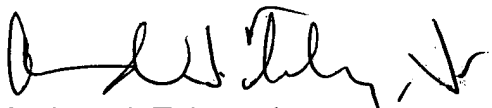

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